Amendments to the Claims

Please amend claims 20, 36, 37 and 38 as shown below to correct minor informalities.

Claim 1 (canceled)

Claim 2 (previously presented): The video graphics display engine of claim 4 wherein the video graphics display engine allocates a size of the first memory block of the single frame buffer and a size of the second memory block of the single frame buffer based on needs of the video data and the graphics data, respectively, and wherein the video graphics display further comprises a controller operably coupled to the video scaler and the graphics scaler, wherein the controller provides control information to the video scaler and the graphics scaler, wherein scaling operations of the video scaler and the graphics scaler utilize the control information.

Claim 3 (original): The video graphics display engine of claim 2, wherein the merging block is operably coupled to the controller, wherein the merging block receives merging control information from the controller, wherein the merging control information is used with the scaled video stream data and the scaled graphics stream to produce the video graphics output stream.

Claim 4 (previously presented): A video graphics display engine comprising:

a video scaler adapted to receive a video data stream in a first format, wherein the video scaler scales video images in the video data stream based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive a graphics data stream in a second format,

wherein the graphics scaler scales graphics images in the graphics data stream based on a ratio between the graphics images in the second format and an output graphics image to produce a scaled graphics stream;

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce a video graphics output stream; and

a single frame buffer operably coupled to the graphics scaler and to the video scaler, the single frame buffer further comprises a first memory block and a second memory block, wherein the stream of video data is fetched from the first memory block and the stream of graphics data is fetched from the second memory block.

Claim 5 (canceled)

Claim 6 (previously presented): The display engine of claim 4, wherein the controller further comprises a video controller operably coupled to a graphics controller,

wherein the video controller is operably coupled to the video scaler, wherein the video controller provides a first portion of the control information to the video scaler,

wherein the graphics controller is operably coupled to the graphics scaler, wherein the graphics controller provides a second portion of the control information to the graphics scaler, and

wherein the video controller and the graphics controller are synchronized.

Claim 7 (previously presented): The display engine of claim 4, wherein the merging block performs an alpha blend operation on the scaled video stream and the scaled graphics stream to produce the video graphics output stream.

Claim 8 (previously presented): The display engine of claim 4 further comprises a digital to analog converter operably coupled to the merging block, wherein the digital to analog converter converts the video graphics output stream to an analog display signal.

Claim 9 (previously presented): The display engine of claim 4 further comprises a display driver operably coupled to the merging block, wherein the display driver is adapted to receive the video graphics output stream in digital format, wherein the display driver formats the video graphics output stream in a display compatible format.

Claim 10 (previously presented): The display engine of claim 4 further comprises a display driver operably coupled to the video scaler, wherein the display driver is adapted to

receive the scaled video stream and produce a video display output based on the scaled video stream.

Claim 11 (previously presented): The display engine of claim 4 further comprises a display driver operably coupled to the graphics scaler, wherein the display driver is adapted to receive the scaled graphics stream and produce a graphics display output based on the scaled graphics stream.

Claim 12 (previously presented): The display engine of claim 4 further comprises a graphics flicker removal block operably coupled to the graphics scaler, wherein the graphics flicker removal block removes flicker from the scaled graphics stream.

Claim 13 (previously presented): The display engine of claim 4 further comprises a video flicker removal block operably coupled to the video scaler, wherein the video flicker removal block removes flicker from the scaled video stream.

Claim 14 (previously presented): The display engine of claim 4 further comprises a plurality of graphics scalers, wherein each of the plurality of graphics scalers receives the graphics data stream and scales the graphics images in the graphics data stream based on a ratio between the graphics images in the second format and a corresponding output graphics image to produce a corresponding scaled graphics stream.

Claim 15 (previously presented): The display engine of claim 4, wherein the merging block further comprises circuitry which configures a pixel rate of the video graphics output stream to produce a preferred video scaling ratio, wherein the preferred video scaling ratio is based on the ratio between the video images in the first format and the output video image.

Claim 16 (previously presented): The display engine of claim 4, wherein the merging block further comprises circuitry which configures a pixel rate of the video graphics output stream to produce a preferred graphics scaling ratio, wherein the preferred graphics scaling ratio

is based on the ratio between the graphics images in the second format and the output graphics image.

Claim 17 (previously presented): The display engine of claim 4 further comprises a video decompression block operably coupled to the video scaler, wherein the video decompression block receives a compressed stream of video data and decompresses the compressed stream of video data to produce the video data stream.

Claim 18 (previously presented): The display engine of claim 4 further comprises a graphics decompression block operably coupled to the graphics scaler, wherein the graphics decompression block receives a compressed stream of graphics data and decompresses the compressed stream of graphics data to produce the graphics data stream.

Claim 19 (previously presented): The display engine of claim 4, wherein the video data stream is a decoded MPEG data stream.

Claim 20 (currently amended): A method for displaying video graphics data comprising:

receiving a video data stream, wherein the video data stream includes video data in a first format;

allocating a first block of a memory in a frame buffer for storing the video data stream, the allocating based upon memory needs of the video data stream;

receiving a graphics data stream, wherein the graphics data stream [of] includes graphics data in a second format;

allocating a second block of the memory in a frame buffer for storing the graphics data stream, the allocating based upon memory needs of the graphics data stream;

scaling the video data based on a ratio between the first format and a selected video format to produce a scaled video stream;

scaling the graphics data based on a ratio between the second format and a selected graphics format to produce a scaled graphics stream; and

merging the scaled video stream and the scaled graphics stream to produce a video graphics output stream.

Claim 21 (original): The method of claim 20, wherein scaling the video data further comprises scaling the video data based on video data control information, and wherein scaling the graphics data further comprises scaling the graphics data based on graphics data control information.

Claim 22 (original): The method of claim 20, wherein merging further comprises receiving merging control information, wherein the merging control information is used in merging scaled video stream and the scaled graphics stream to produce the video graphics output stream.

Claim 23 (original): The method of claim 20, further comprises converting the video graphics output stream to an analog format.

Claim 24 (original): The method of claim 20, wherein scaling the video data further comprises removing the flicker from the scaled video stream.

Claim 25 (original): The method of claim 20, wherein scaling the video data further comprises removing the flicker from the scaled graphics stream.

Claim 26 (original): The method of claim 20, wherein scaling the video data further comprises scaling the video data based on the first format and a plurality of selected video formats to produce a plurality of scaled video streams.

Claim 27 (original): The method of claim 20, wherein scaling the graphics data further comprises scaling the graphics data based on the first format and a plurality of selected graphics formats to produce a plurality of scaled graphics streams.

Claim 28 (original): The method of claim 20, wherein receiving the video data stream further comprises receiving the video data stream in a compressed format, wherein the video data stream is decompressed prior to scaling.

Claim 29 (original): The method of claim 20, wherein receiving the graphics data stream further comprises receiving the graphics data stream in a compressed format, wherein the graphics data stream is decompressed prior to scaling.

Claim 30 (original): A video graphics integrated circuit comprising:

a frame buffer, wherein the frame buffer stores video data and graphics data;

a video scaler operably coupled to the frame buffer, wherein the video scaler scales the video data to produce a scaled video stream;

a graphics scaler operably coupled to the frame buffer, wherein the graphics scaler scales the graphics data to produce a scaled graphics stream; and

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the sealed video data stream and the graphics data stream to produce a video graphics output stream.

Claim 31 (previously presented): A video graphics circuit comprising:

a plurality of memory blocks, wherein each of the plurality of memory blocks stores at least one of video data and graphics data;

a plurality of video scalers, wherein each of the plurality of video scalers is coupled to at least one of the plurality of memory blocks, wherein each video scaler of the plurality of video scalers independently scales at least a portion of the video data to produce a scaled video data stream of a plurality of scaled video data streams independent from the other scaled video data streams of the plurality of scaled video data streams;

a plurality of graphics scalers, wherein each of the plurality of graphics scalers is coupled to at least one of the plurality of memory blocks, wherein each graphics scaler of the plurality of graphics scalers independently scales at least a portion of the graphics data to produce a scaled graphics data stream of a plurality of scaled graphics data streams independent from the other scaled graphics data streams of the plurality of scaled graphics data streams; and

a plurality of merging blocks, wherein each of the merging blocks is operably coupled to at least one video scaler of the plurality of video scalers and at least one graphics scaler of the plurality of graphics scalers such that each of the merging blocks receives a plurality of scaled data streams, wherein each merging block combines received scaled data streams to produce a video graphics output stream of a plurality of video graphics streams.

Claim 32 (previously presented): The video graphics circuit of claim 31, wherein the plurality of video scalers, the plurality of graphics scalers, and the plurality of merging bocks are included in an integrated circuit.

Claim 33 (previously presented): The video graphics circuit of claim 32, wherein at least a portion of the plurality of memory blocks is included in the integrated circuit.

Claim 34 (previously presented): The video graphics circuit of claim 31 further comprises a plurality of controllers, wherein each of the plurality of controllers is operably coupled to at least one scaler of a combined set of scalers that includes the plurality of graphics scalers and the plurality of video scalers, wherein each of the plurality of controllers provides separate control information that controls independent scaling by scalers to which it is coupled.

Claim 35 (previously presented): The video graphics circuit of claim 34, wherein each of the plurality of controllers provides merging control information to one of the plurality of merging blocks, wherein the merging control information is used in combining the received scaled data stream by each merging block.

Claim 36 (currently amended): The video graphics circuit of claim 31, wherein each of the plurality of merging blocks perform alpha blend operations [in] to combine the received scaled data streams.

Claim 37 (currently amended): The video graphics circuit of claim 31, wherein the plurality of merging blocks produces the plurality of video graphics output streams in at least one of an analog display format and a digital display format.

Claim 38 (currently amended): A video graphics display circuit, comprising:

a frame buffer memory maintaining video data having a first format and graphics data having a second format, wherein the frame buffer memory allocated to the video data and the graphics data is based upon memory needs of the video data and the graphics data;

a video scaler adapted to receive the video data, wherein the video scaler scales video images in the video data based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive the graphics data, wherein the graphics scaler scales graphics images in the graphics data based on a ration between the graphics images in the second format and an output graphics image to produce a scaled graphics stream, the video image scaling being independent of the graphics image scaling; and

a merging block operatively coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce a[n] video graphics output stream.